

**UNITED STATES PATENT APPLICATION FOR:**  
**METHOD AND TEST DEVICE FOR DETERMINING A REPAIR SOLUTION FOR A**  
**MEMORY MODULE**

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**ATTORNEY DOCKET NUMBER: INFN/0058**

**CERTIFICATION OF MAILING UNDER 37 C.F.R. 1.10**

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February 20, 2004  
Date of signature

## **METHOD AND TEST DEVICE FOR DETERMINING A REPAIR SOLUTION FOR A MEMORY MODULE**

### **CROSS-REFERENCE TO RELATED APPLICATIONS**

[0001] This application claims foreign priority benefits under 35 U.S.C. §119 to co-pending German patent application number 103 07 027.3, filed February 20, 2003. This related patent application is herein incorporated by reference in its entirety.

### **BACKGROUND OF THE INVENTION**

#### **Field of the Invention**

[0002] The invention relates to a method for determining a repair solution for a memory module in a test system. The invention furthermore relates to a test device for determining a repair solution for a memory module which can be connected to the test device.

#### **Description of the Related Art**

[0003] Memory module, in particular memory modules having dynamic memory cells, DRAMs, cannot be fabricated without defects. Thus, after the fabrication of the memory modules, there are always some defective memory cells among the memory cells. In order to be able to repair these defective memory cells, additional memory cells are provided on the memory module. These additional memory cells are called redundant memory cells.

[0004] After the memory module has been fabricated, the functioning of the individual memory cells is checked. By writing to and reading from a memory cell, it is possible in this case to identify defective memory cells. The defect in a memory cell is identified by comparing the datum written in with the datum read out, a defect being identified if the datum written in and the datum read out differ from one another. The comparison between the written and read-out data can be effected both in the memory module itself and in the test system.

[0005] The comparison data thus generated are called defect data and specify whether a defect is present in a memory cell. It is often the case that only memory areas having a plurality of memory cells can be replaced by redundant memory areas, so that it suffices for a defect datum to specify whether a defect is present in the memory area. The volume of defect data is thereby reduced.

[0006] The test sequence is essentially controlled by a test device containing a defect address memory in which the defect data determined are stored. The defect address memory is essentially a mapping of the memory cell array, a memory location of the defect address memory mapping a memory cell or a memory area having a plurality of memory cells of the memory module. A bit which is set in a memory location of the defect address memory then corresponds to one or a plurality of defective memory cells in the memory module. If the bit is not set, then no defect is present.

[0007] The defect address memory serves as a basis for the redundant calculation which is used to perform a replacement of the defective memory cells by a disconnection of the defective memory areas and an activation of redundant memory elements. Memory elements may be, by way of example, word line groups comprising one or a plurality of word lines or bit line groups comprising one or a plurality of bit lines. Since the defect address memory stores the defect data for all the memory areas, that is to say also for functional memory areas, a large defect address memory is necessary in the case of parallel testing of a plurality of memory modules with a large storage capacity. Said defect address memory must have fast access times in order not to reduce the test speed and thus to increase the throughput of the test system.

### **SUMMARY OF THE INVENTION**

[0008] It is an object of the present invention to provide a test method, a test device and a test system in which the size of the defect address memory can be reduced.

[0009] This object is achieved by means of the methods according to claims 1 and 18, by means of the test device according to claim 7, by means of the test systems according to claim 15.

[0010] Further advantageous refinements of the present invention are specified in the dependent claims.

[0011] A first aspect of the present invention provides a method for determining a repair solution for a memory module in a test system. Memory areas comprising one or a plurality of memory cells are successively tested in order to obtain, for each memory area, a defect datum which specifies whether the respective memory area is defective. Defect addresses, the address values of which specify the defective memory areas of the memory module, are generated from the addresses of the memory areas and the associated defect data. The defect addresses are stored in the test system, the repair solution being determined from the stored defect addresses.

[0012] The method according to the invention has the advantage that the memory size of the defect memory can be chosen to be significantly smaller than heretofore. Conventional test systems are provided with a defect data memory which essentially provides a memory location for each memory area, a defect datum being stored in said memory location. Thus, by way of example, a logic "0" is stored in the memory location if the corresponding memory area in the tested memory module is free of defects. A logic "1" is stored if a defect occurred during the testing of the corresponding memory area.

[0013] By contrast, in the case of the invention, it is now provided that when a defect occurs in a memory area of the memory module to be tested, the address of the memory area is determined and said address is stored in the defect address memory of the test device. Since the number of defective memory areas in a memory module is usually relatively small compared with the total number of memory areas or it is possible to repair only a small number of defective memory areas in the memory module, the size of such a defect address memory can be chosen to be significantly smaller than the size of the conventional defect data memory. Since only the defect

addresses are necessary for calculating the repair solution, the information about defect-free memory areas can be discarded.

[0014] It may furthermore be provided that the memory areas in each case have one or a plurality of memory cells which can be addressed in each case via a word line group – assigned to the address – comprising one or a plurality of word lines and via a bit line group – assigned to the address – comprising one or a plurality of bit lines. The repair solution specifies whether a defective memory area is to be repaired by a replacement of the corresponding word line group by a redundant word line group comprising one or a plurality of redundant word lines or by a replacement of the corresponding bit line group by a redundant bit line group comprising one or a plurality of redundant bit lines.

[0015] A number of defective memory areas is mandatorily marked as to be replaced by a redundant word line group if the defective memory areas can be addressed by a common word line group and the number exceeds a first maximum number. A number of defective memory areas is mandatorily marked as to be replaced by a redundant bit line group if the defective memory areas can be addressed by a common bit line group and the number exceeds a second maximum number. The memory areas which are thereby already marked as to be replaced are taken into consideration in the further determination of the redundancy solution by said marked memory areas being assigned an available redundant word line group or an available redundant bit line group.

[0016] What is thereby advantageously achieved is that the calculation of the repair solution is simplified by virtue of the fact that defective memory areas, which in any case can only be replaced by a redundant word line group or a redundant bit line group, are marked as to be replaced by the latter. This is done as early as during the determination of the defect addresses. Only the memory areas which have not yet been identified as to be replaced by the redundant word line groups or bit line groups are taken into consideration for the further calculation of the repair solution. This considerably simplifies the method for determining the repair solution since generally

a smaller number of defect addresses have to be taken into consideration in the further course of determining the repair solution.

[0017] Preferably, the first maximum number corresponds to the number of available redundant bit line groups and/or the second maximum number corresponds to the number of available redundant word line groups. The word line groups or bit line groups would thus be marked as to be replaced, before the actual determination of the repair solution, if there is no other possibility for replacing the corresponding defective memory areas.

[0018] A further aspect of the present invention provides a test device for determining a repair solution for a memory module which can be connected to the test device. The test device has a control unit in order to carry out a test operation for memory areas in the memory module. A memory unit is furthermore provided in order to store a value of a defect address which specifies which address of a memory area of the memory module is defective. Furthermore, an evaluation unit is provided, in order to determine the repair solution from the stored defect addresses. The connectable memory module comprises memory areas which in each case have one or a plurality of memory cells. The memory areas can be addressed in each case via a word line group – assigned to the address – comprising one or a plurality of word lines and via a bit line group – assigned to the address – comprising one or a plurality of bit lines. The repair solution specifies whether a defective memory area is to be repaired by a replacement of the corresponding word line group by a redundant word line group comprising one or a plurality of redundant word lines or by a replacement of the corresponding bit line group by a redundant bit line group comprising one or a plurality of redundant bit lines.

[0019] In this way, a test device is provided which, depending on the number of defects occurring, manages with a considerably smaller memory requirement for the defect address memory than conventional test devices. By virtue of the fact that only the defect addresses are stored, which specify the defective memory areas, and a mapping of the entire memory of the memory module in the defect data memory of

the test system is not performed, memory space for the defect memory can be saved to a considerable extent.

[0020] Preferably, each word line group is assigned a first memory segment having a first number of defect address memory locations, in order to store an identified defect address in the corresponding first memory segment of the word line group by means of which the defective memory area can be addressed. Each bit line group is preferably assigned a second memory segment having a second number of defect address memory locations, in order to store an identified defect address in the corresponding second memory segment of the bit line group by means of which the defective memory area can be addressed. The first number corresponds to the number of redundant bit line groups present, and the second number corresponds to the number of redundant word line groups present.

[0021] In this way, it is possible to configure the memory unit in the test device in such a way that an assignment of memory locations to word line groups and bit line groups in the memory module to be tested has already been effected beforehand. This enables faster addressing of the defect address memory. Furthermore, it makes it possible to identify, by means of an overflow of the defect address memory locations assigned to a word line group or to a bit line group, that the respective word line group or the respective bit line group is to be replaced by a redundant word line group or a redundant bit line group.

[0022] Preferably, during the determination of the repair solution, the evaluation unit unconditionally defines an available redundant word line group as repair solution for the defective memory areas which can be addressed via a word line group, if the first number exceeds the number of redundant bit line groups present. The evaluation unit unconditionally defines a redundant bit line group for the defective memory areas which can be addressed via a bit line group, if the second number exceeds the number of redundant word line groups present.

[0023] In this way, without complex calculation, the evaluation unit already establishes beforehand the memory areas which are always to be replaced by an available word line group or a bit line group. Defective memory areas which can only

be repaired with the aid of a redundant word line group anyway for lack of a sufficient number of redundant bit line groups are marked as "to be repaired by a redundant word line group". Equally, memory areas which can only be repaired with a redundant bit line for lack of a redundant word line group present are marked as "to be repaired by a redundant bit line".

[0024] In the course of the further determination of the repair solution, the defect addresses of the word line and/or bit line groups to be unconditionally replaced are not taken into consideration in the determination of the repair solution with regard to the defect addresses which have remained. A redundant word line group or bit line group is allocated only to the memory areas marked as to be repaired unconditionally by a redundant word line group or bit line group. As a result, the method for determining the repair solution is considerably shortened, since often fewer defect addresses are to be taken into consideration.

[0025] Preferably, the test device may have a converter circuit in order to convert defect data assigned to memory areas into defect addresses by the defect address being determined by that address of the memory area at which a defect has been identified. Such a test device receives defect data assigned to corresponding memory areas. The defect data specify whether or not a defect occurred in the respective memory area. By virtue of the fact that the converter circuit is provided in the test device, it is possible to dispense with such a circuit in the memory module.

[0026] As an alternative, such a converter circuit may also be provided in a memory module, so that the data to be transmitted to the test device can be considerably minimized since only the defect addresses and not information about defect-free memory areas are transmitted.

[0027] A further aspect of the present invention provides a test system having a test device according to the invention and a memory module.



### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0028] Preferred embodiments of the invention are explained in more detail below with reference to be accompanying drawings, in which:

[0029] Figures 1A, 1B show test system according to the prior art;

[0030] Figure 2 shows an illustration of the defect data memory mapping the memory cell array of the memory module;

[0031] Figures 3A, 3B show an illustration for different possibilities for replacing defective memory areas;

[0032] Figures 4A, 4B show embodiments for a test system according to the present invention;

[0033] Figure 5 shows an illustration of the assignment of the memory locations of the memory unit in a test system according to the invention; and

[0034] Figures 6A, 6B show a flow diagram for illustrating the method according to the invention.

### **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

[0035] Figure 1A illustrates a test system according to the prior art. The test system has a test device 1, to which a memory module 2 to be tested is connected. The test device 1 makes address data available, which are made available to the memory module 2 to be tested via address lines 3. Via data lines 4, data to be written to the memory cells of the memory module to be tested and also the data read from the memory cells are transmitted between the memory module 2 and the test device 1.

[0036] During testing, test data are written to the memory cell of the memory module 2 in accordance with the address prescribed via the address lines 3. Afterward, the written data are read out again via the data lines 4 and the test data written in and the test data subsequently read out again are compared with one another in a comparator circuit 5. If a deviation is established, then the relevant memory cell is defective.

[0037] The test device 1 furthermore has a defect data memory, which is essentially a mapping of the memory to be tested in the memory module 2. It may be provided then, that the defect data memory 6 in the test device 1 essentially has the same size as the memory in the memory module 2 to be tested. The defect data produced as a result of the comparison in the comparator device 5 are stored in the defect data memory 6 in such a way that each memory location of the defect data memory 6 is assigned to an address of a memory cell of the memory module 2.

[0038] A repair solution is then determined from the defect data stored in the defect data memory 6, which repair solution specifies which redundant memory elements are to replace the relevant defective memory cell. Since the redundant memory elements often comprise one or a plurality of redundant word lines or one or a plurality of redundant bit lines, it suffices for a defect data to specify whether at least one of the memory cells of a memory area which can be replaced by a redundant memory area is defective. In this case, the defect data memory 6 may be smaller than the memory to be tested of the memory module 2. This is because there only a respective defect datum is provided for a memory area, which may have a plurality of memory cells. The defect information is compressed in a redundancy-conforming manner in this way.

[0039] Fig 1B illustrates a further possibility of a test system. In this case, the comparator circuit 5 is already integrated in the memory module 2, so that only the defect data has to be transmitted to the test device 1 via a corresponding defect data line 7.

[0040] Figure 2 illustrates how the defect data memory represents a mapping of the memory of the memory module 2. It can be seen that a defect in a memory cell which has occurred in the memory array of the memory module 2 brings about a storage of a corresponding defect datum indicating a defect, e.g. of a logic "1" in the defect data memory 6. A defect file indicating a defect may also be indicated by a logic "1". The hatched circles in the memory of the memory module 2 specify a defective memory cell or a defective memory area. The hatched circles in the defect

data memory 6 indicate defect data which indicate a defect in the relevant memory area of the memory module 2, e.g. a logic "1".

[0041] Figure 3A illustrates how, by way of example, four defective memory areas lying along a word line WL can be replaced. A memory cell array 10 is taken as a basis in this case, by way of example, four redundant word line groups 12 and four redundant bit lines groups 11 being provided in the memory module 2 to be tested. A word line group comprises 1 or a plurality of word lines and a bit line group comprises 1 or a plurality of bit lines. The size of the word line group or of the bit line group depends on the intended size of the memory areas that are in each case to be replaced. A word line group in the memory cell array 10 is thus replaced by a redundant word line group of the same size, and a bit line group in the memory cell array 10 is likewise replaced by a redundant bit line group of the same size.

[0042] The number of redundant word line groups and redundant bit line groups is defined for a predetermined memory module but is essentially freely selectable and determined by the probability of occurrence of defects in the memory cell array. Generally, each defect in a memory area may be corrected by the replacement of the relevant memory area by a redundant word line group or a redundant bit line group. In the case shown the four defective memory areas which can be addressed via a word line group may be replaced by a redundant word line group or four redundant bit line groups.

[0043] If the number of defective memory areas arranged along a word line group is larger than the number of available redundant bit line groups, these defective memory areas, as illustrated in Figure 3B, can be completely replaced only by a redundant word line group, but not by redundant bit line groups, since there are not enough redundant bit line groups present.

[0044] Thus, if the number of defective memory areas along a word line group or a bit line group does not exceed the number of available redundant bit lines groups or redundant word line groups, then the repair solution is not unambiguous and must be determined in accordance with known methods for determining the repair solution. If the number of defective memory areas along a word line group or along a bit line

group exceeds the number of available redundant bit line groups or redundant word line groups, then the corresponding word line groups must be replaced by a redundant word line group or the bit line group must be replaced by a redundant bit line group.

[0045] Figure 4A illustrates a first embodiment of a test system according to the invention. A memory module 21 to be tested is connected to a test device 20 via address lines 22 and data lines 23. For the testing of the memory module 21, the test device 20 makes test addresses available via the address lines 22 and also makes test data available via the data lines 23.

[0046] In a comparator device 24, the data written in and subsequently read out again are compared and defect data are made available to a converter circuit 25, in which a defect address FA is generated with the aid of the respectively tested address and the defect datum determined, which defect address is stored in a defect address memory 26. The test operation and also the generation of test patterns is carried out in a test control unit 27. If a test circuit is provided in the memory module 21, the test addresses and test data are generated in the memory module 21, so that the test control unit 27 may be obviated.

[0047] The second embodiment of the test system according to the invention is illustrated in Figure 4B. The second embodiment differs from the first embodiment essentially by the fact that the comparator circuit 24 is not provided in the test device 20, but rather is provided as second comparator circuit 28 in the memory module 21 to be tested. In this way, it is possible to save data lines for the transmission of the read-out test data, since only the defect data generated by the second comparator circuit 28 provided in the memory module 21 to be tested has to be transmitted to the test device 20.

[0048] The defect address memory 26 is connected to an evaluation unit 29, which determines a repair solution from the defect addresses determined. The evaluation unit 29 may be embodied either in the test device 20 or separately from the test device 20.

[0049] Figure 5 illustrates the construction of a defect address memory as is to be used in the test system according to the invention. The defect address memory 26 is segmented, each of the word line groups WLG in the memory module 21 being assigned a first memory segment 30 in the defect address memory 26 and each of the bit line groups of the memory module 21 being assigned a second memory segment 31 of the defect address memory 26. The first memory segments 30 have a number of address memory locations corresponding to the number of available redundant bit line groups. The second memory segments 31 have a number of address memory locations corresponding to the number of available redundant word line groups.

[0050] By virtue of the fact that the defect address memory 26 is of segmented design in this form, a defined memory area in the defect memory 26 is available for each of the word line groups and each of the bit line groups of the memory module to be tested, so that an allocation of a memory area when a defect address is present does not have to be effected. This leads to a time saving when storing the defect addresses.

[0051] Furthermore, the defect address memory 26 may be designed such that, in the event of an attempted storage in a defect address in one of the first or second memory segments 30, 31, an overflow of the respective memory segment 30, 31 has the effect that a first or second replacement register 32, 33, the replacement register 32, 33 provided for each of the first and second memory segments 30, 31 of the defect address memory 26 is set to a value which indicates that the respective word line group WLG or bit line group BLG assigned to the respective memory 30, 31 must in any event be replaced by a redundant word line group or redundant bit line group.

[0052] During the determination of the repair solution, firstly the memory segments whose assigned replacement registers 32, 33 are set are allocated in each case redundant word line groups or a redundant bit line group. If a replacement register 32, 33 is set, then the word line group assigned to the corresponding memory segment is replaced by a corresponding available redundant word line group and the

bit line group assigned to the corresponding memory segment is replaced by an available redundant bit line group. The further determination of the repair solution is then carried out only with regard to the defect addresses which are stored in the first and second memory segments 30, 31 whose assigned replacement register 32, 33 has not been set.

[0053] Figures 6A and 6B illustrate a flow diagram for an embodiment of the method according to the invention. It relates to the storage of the defect addresses and also to the setting of the replacement registers 32, 33 in the defect address memory 26. In step S1, defect data are determined, which are the result of a comparison of the test data written to the memory cell array and the data subsequently read out. If a defect is indicated by the defect datum, then the tested memory area address respectively assigned to the defect is generated as a defect address in a step S2.

[0054] Afterward, in a step S3, the memory segments 30, 31 are provided, which are assigned to the respective word line group or bit line group which address the defective memory area. In a step S4, the defect address determined and the defect addresses stored in the first memory segment are compared with one another. If, in a step S5, it is established that the defect address determined is a new defect address which has not yet been stored in the assigned first memory segment 30, the defect address determined is added to the memory segment (S6). In a step S7, a check is made to determine whether the added defect address leads to an overflow of the first memory segment 30. If so, the first replacement register 32 is set in a step S8.

[0055] Afterward, the defect address determined is compared, in a step S9, with the defect addresses stored in the second assigned memory segment. If a defect is established in a step S10, the defect address determined is added, in a step S11, to the defect addresses stored in the memory segment. If the addition of the defect address to the second memory segment leads to an overflow (step S12), then the second replacement register 33 is set (step S13).

[0056] If, in step S10, it was established that the defect address is already stored in the second memory segment, the method jumps back to step S1.

[0057] If no new defect address is found in step S10 or if the second replacement register is set in step S13, then firstly a check is made, in a step S14, to determine whether further defect data which are to be stored are present. If so, the method jumps back to step S1. If not, firstly the word line groups and bit line groups marked by a set first and/or second replacement register 32, 33 are allocated redundant word line groups or bit line groups and the part of the repair solution is subsequently determined using the defect addresses which remained after the replacement of the word line groups or bit groups already determined (step S15).

[0058] The method described above may also provide for only the first memory segments 30 or only the second memory segments to be provided, so that only word line groups or only bit lines groups are determined for replacement before the repair solution is determined with the remaining defect addresses stored in the defect address memory.